AMENDMENTS TO THE CLAIMS

1. (currently amended) A protective structure for blocking the propagation of defects generated in a semiconductor device, the structure comprising:

a plurality of deep trench isolations formed between a memory storage region of the semiconductor device and a logic circuit region of the semiconductor device, said plurality of deep trench isolations being filled with an insulative material;

said plurality of deep trench isolations further comprising an inner perimeter and an outer perimeter, wherein individual deep trench isolations included in said outer perimeter are disposed adjacent to gaps in between individual deep trench isolations included in said inner perimeter; and

wherein said plurality of deep trench ~~isolation prevents~~ isolations prevent the propagation of crystal defects generated in said logic circuit region from propagating into said memory storage region.

2. (currently amended) The structure of claim 1, wherein each of said plurality of deep trench ~~isolation is~~isolations are formed beneath a corresponding shallow trench isolation, said shallow trench isolation for electrically isolating devices contained in said memory storage region from devices contained in said logic circuit region.

3. (currently amended) The structure of claim 1, ~~further comprising a~~ wherein said plurality of deep trench isolations surround~~ing~~ said memory storage region.

4. (cancelled)

5. (original) The structure of claim 1, wherein said memory storage region comprises a DRAM array region.

6. (original) The structure of claim 1, wherein said memory storage region

comprises a DRAM array region.

7. (original) The structure of claim 6, wherein said logic circuit region further includes:

a plurality of CMOS devices; and

a high dose impurity layer implanted within a substrate of said logic circuit region, said high dose impurity layer used to inhibit parasitic bipolar transistor action between said plurality of CMOS devices.

8. (currently amended) An embedded DRAM (eDRAM) device, comprising:

a logic circuit region;

a memory storage region embedded ~~within~~ adjacent said logic circuit region;

a shallow trench isolation for electrically insulating devices included within said memory storage region from devices included within said logic circuit region; ~~and~~

a plurality of deep trench isolations, formed underneath said shallow trench isolation, said plurality of deep trench isolations for preventing the propagation of crystal defects generated in said logic circuit region from propagating into said memory storage region; and

said plurality of deep trench isolations further comprising an inner perimeter and an outer perimeter, wherein individual deep trench isolations included in said outer perimeter are disposed adjacent to gaps in between individual deep trench isolations included in said inner perimeter.

9. (original) The eDRAM device of claim 8, wherein said shallow trench isolation surrounds said memory storage region.

10. (currently amended) The eDRAM device of claim 9, ~~further comprising a~~ wherein said plurality of deep trench isolations surround~~ing~~ said memory storage region.

11. (cancelled)

12. (currently amended) The eDRAM device of claim 11, wherein said memory storage region includes a plurality of deep trench storage capacitors.

13. (original) The eDRAM device of claim 12, wherein said logic circuit region further includes:

a plurality of CMOS devices; and

a high dose impurity layer implanted within a substrate of said logic circuit region, said high dose impurity layer used to inhibit parasitic bipolar transistor action between said plurality of CMOS devices.

14. (withdrawn) A method for blocking the propagation of defects generated in a semiconductor device, the method comprising:

forming a deep trench isolation formed between a memory storage region of the semiconductor device and a logic circuit region of the semiconductor device; said deep trench isolation being filled with an insulative material;

wherein said deep trench isolation prevents the propagation of crystal defects generated in said logic circuit region from propagating into said memory storage region.

15. (withdrawn) The method of claim 14, wherein said deep trench isolation is formed beneath a shallow trench isolation, said shallow trench isolation for electrically isolating devices contained in said memory storage region from devices contained in said logic circuit region.

16. (withdrawn) The method of claim 14, further comprising forming a plurality of deep trench isolations to surround said memory storage region.

17. (withdrawn) The method of claim 16, further comprising:

configuring said deep trench isolations to form an inner perimeter and an outer perimeter, wherein individual deep trench isolations included in said outer perimeter are disposed adjacent to gaps in between individual deep trench isolations included in said inner perimeter.

18. (withdrawn) The method of claim 14, wherein said memory storage region comprises a DRAM array region.

19. (withdrawn) The method of claim 18, wherein said DRAM array region includes a plurality of deep trench storage capacitors.

20. (withdrawn) The method of claim 19, wherein said logic circuit region further includes:

a plurality of CMOS devices; and

a high dose impurity layer implanted within a substrate of said logic circuit region, said high dose impurity layer used to inhibit parasitic bipolar transistor action between said plurality of CMOS devices.